Composable Code Generation for Distributed Giotto

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Compositionality Seminar WS 2007 Department of Computer Sciences University of Salzburg

Motivation

Automotive software

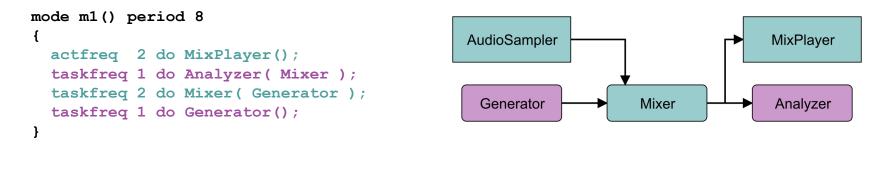
- Suppliers develop software components
- Manufacturer integrates components
 - Mass production: optimality
- Compositional design
 - Scale down problem
 - Reuse components
 - Preserve desired properties by composition

Real Time + Composability

- Giotto framework
 - Purely software time-triggered paradigm
 - Concurrency abstraction: Logical Execution Time
 - Enables compositional design of hard real-time systems
- Distributed platform
 - Realized by distributed compilation of components
 - Individually compiled components merged to final program
- Merge & Verification
 - Automatic check if components meet specification

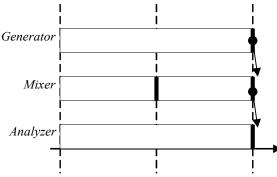
Giotto Framework

- Giotto program
 - Executes a *periodic* set of LET tasks
 - Set of tasks and periods may change upon mode switches



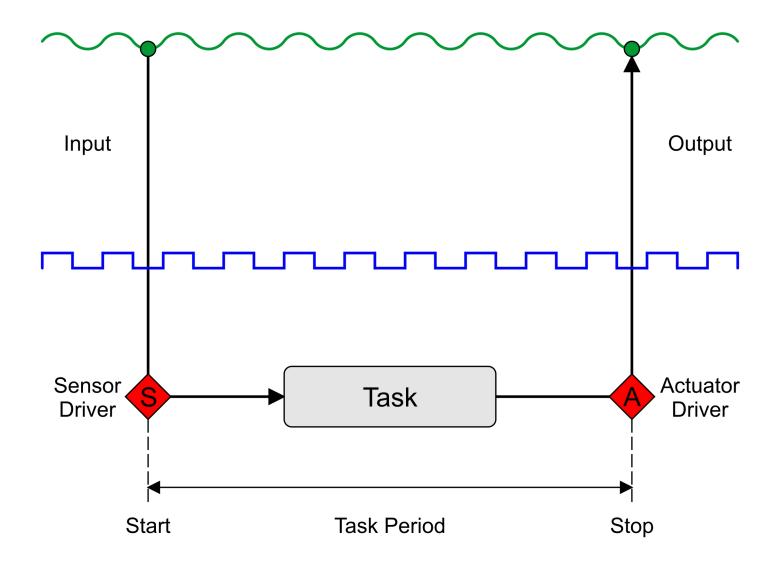
Task instance

 Period defines start and stop times
 Output available at stop time

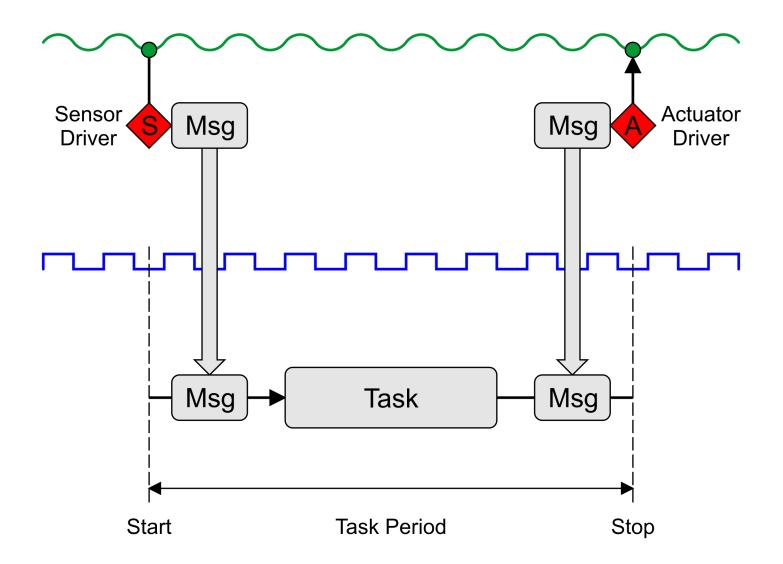


n

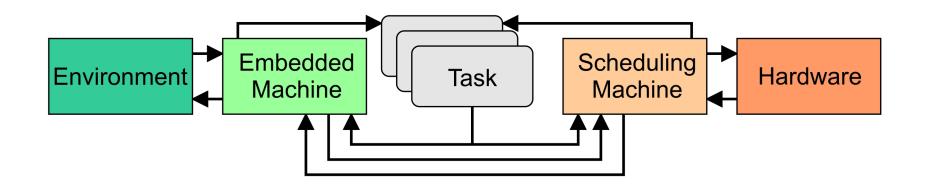
Giotto Abstraction



Giotto Implementation



E and S Machine



- Embedded Machine E code
 - Environment interaction
 - Task release

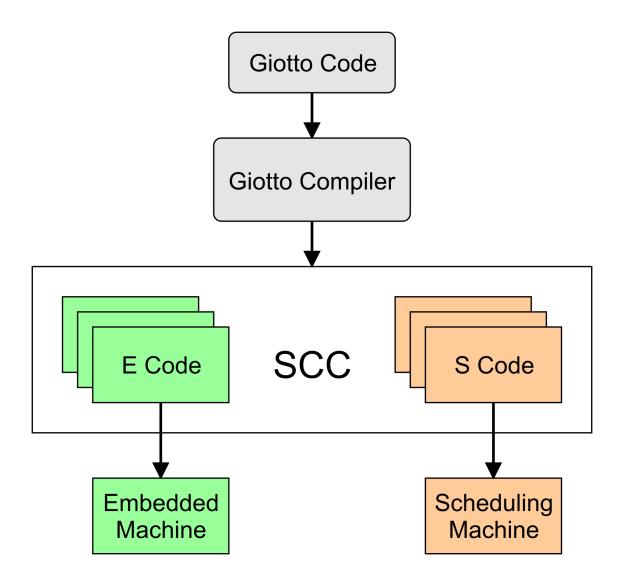
Scheduling Machine - S code

- Task execution
- Communication schedule

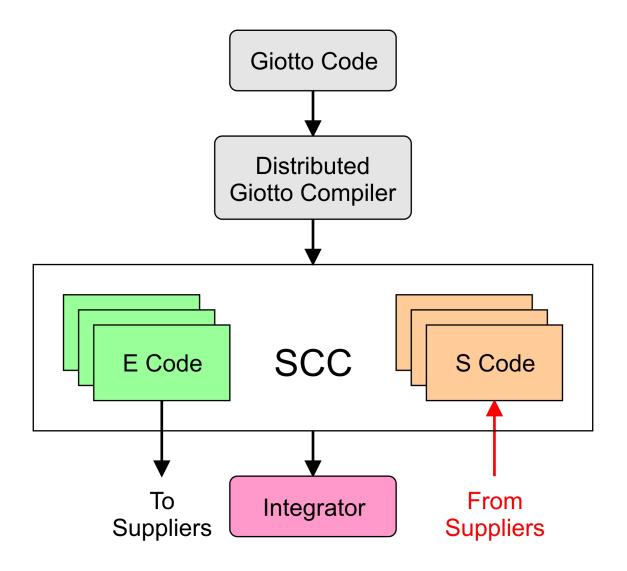
E_{s,h}(m₁, 0): call(copy[MixSound]) call(copy[StringSound]) release(1; Mixer; 1) release(1; [MixSound]) future(4, E_{s,h}(m₁, 1))

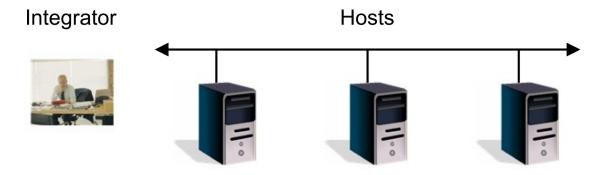
```
S<sub>s,h</sub>( m<sub>1</sub>, 0 ):
idle( 1 )
call( InDrv2 )
dispatch( Mixer; 2 )
idle( 3 )
dispatch( [MixSound]; 4 )
```

Schedule-Carrying Code



Distributed Compilation







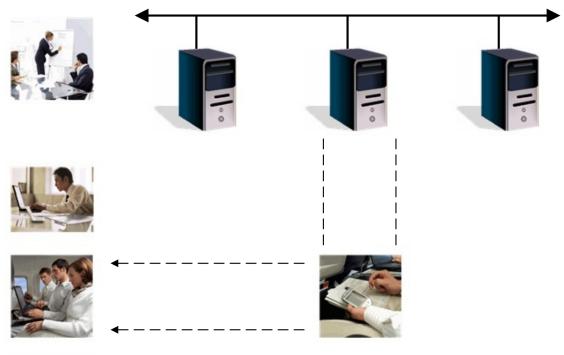




Suppliers

Step 1

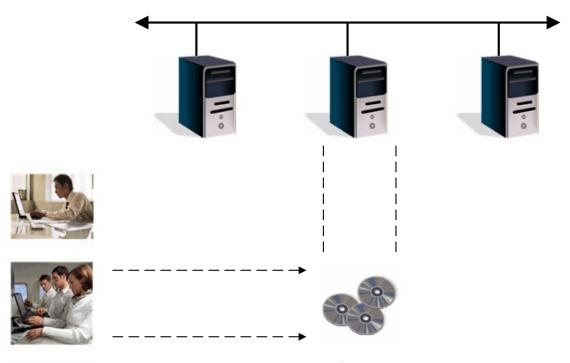
Integrator





Specification (E Code Module and Timing Interface)

Step 2



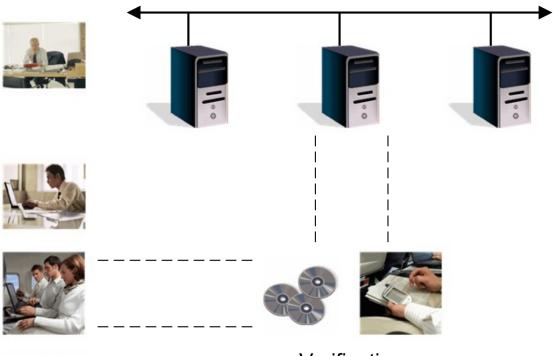


Code (S Code and Task Implementation)

Suppliers

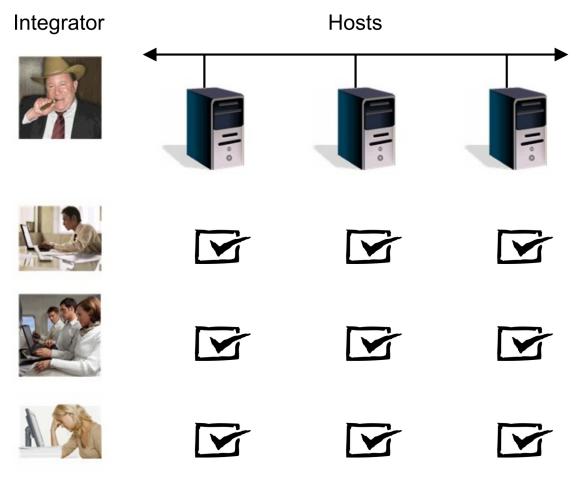
Step 3

Integrator





Verification (S Code vs. Specification)



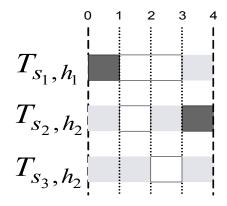
Suppliers

Specification

- Supplier s on host h gets
 - Component specification
 - E code module $E_{s,h}$

 $E_{s,h}(m_1, 0):$ call(copy[MixSound]) call(copy[StringSound]) release(1; Mixer; 1) release(1; [MixSound]) future(4, $E_{s,h}(m_1, 1)$)

- Timing interface
 - Set of time intervals T_{s,h}
 - where s may use h
 - □ where *s* may send



Integrator ensures interface feasibility

Integration

- Integrator receives
 - S code module $S_{s,h}$
 - Even with interfaces EDF optimal
 - Task Implementation
 - Usually written in different language
 - Merged SCC module
 - Time-safe if no driver accesses a released task before completion
 - Complies with timing interface if all tasks executed in time intervals

S_{s,h}(m₁, 0): idle(1) call(InDrv2) dispatch(Mixer; 2) idle(3) dispatch([MixSound]; 4)

Verification

Giotto program G

- \square *n* : bound on all numbers in *G*
- \Box $g_{s,h}$: size of Giotto component implemented by supplier s on host h

Correctness

To check if a distributed SCC program P correctly implements Giotto program G it is enough to check if each $P_{s,h}$ complies to $T_{s,h}$ and is time-safe

Complexity

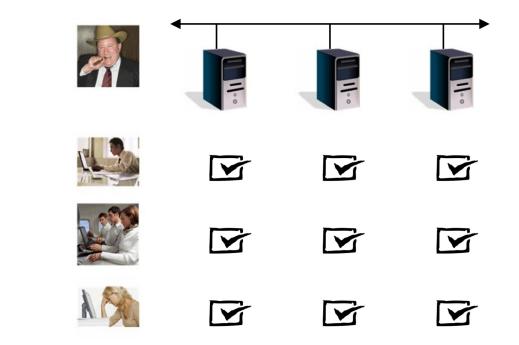
If a given $P_{s,h}$ complies to $T_{s,h}$ and is time-safe can be checked in

 $O(g_{s,h}n)$ time

Verification

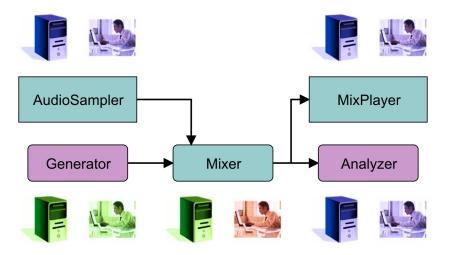
- Module modification
 - Interaction $E_{s,h}$
 - Schedule $S_{s,h}$
 - Duration wcet

 $O(\boldsymbol{g}_{s,h} \boldsymbol{n})$



Implementation

- Distributed audio mixer application
 - □ File read, processed, analyzed, and reproduced
 - Two hosts and three suppliers



- PCs running RT-Linux, Ethernet
 - TDMA on top of software-based synchronization, 2.86Mb/s
 - Every 4ms 44 samples (11kHz) processed and transmitted
 - Overhead 3.7%: synchronization 25μs, virtual machine 12μs

Conclusions

Timing interfaces

- Used to distribute code generation for Giotto programs and distributed target platforms
- Component integration
 - Performed by individually checking interface compliance and time safety of each component

Timing requirements

Guaranteed without solving scheduling problem: burden is shifted to generation of timing interfaces